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METHOD FOR PRODUCING A SILICON-ON-INSULATOR STRUCTURE

Field of the Invention

The invention belongs to semiconductor technology and, more exactly, deals with a method for producing a silicon-on-insulator (SOI) structure.

Description of the Prior Art

A known method for producing a silicon-on-insulator (SOI) structure (US patent no. 5 374 564) implants hydrogen in a first wafer, bonds the first wafer with the second wafer and slices the first wafer. The implantation is realized by ion bombardment of the first wafer to create a layer, which contains hydrogen or inert gas filled micropores near the penetration distance of the ions. This layer divides the wafer into a bottom part that contains the substrate, and the upper part that contains the layer (a thin film) while the tempreature at the hydrogen or inert gas ions is maintained below the temperature at which the gas created by the implanted ions is diffused out of the layer, i.e., between 20 and 450°C. An exfoliation of the bonded wafers is then carried out at a high temperature (e.g., higher than 500°C), which is higher than the temperature of ion implantation and which is enough for a recovery of material structure in the first wafer and for increasing a gas pressure in the micropores . At this time the first and the second wafers are kept in contact. Implantation on the first wafer of one or more layers of different materials with lower penetration depths than the ions is then carried out. The ion implantation is carried out through a silicon dioxide layer as a

buried oxide, and silicon is used for the second wafer.

The method described above has a lot of disadvantages that decrease the quality of the silicon-on-insulator structures produced.

Firstly, there is the low quality of buried oxide in the SOI structures. Namely, the H+ ion implantation is carried out through the silicon dioxide that is used afterward as the buried oxide (BOX). Defects generated during the implantation as well as the implanted hydrogen deteriorate isolation properties of the SiO_2 BOX layer. The insulating properties of the SiO_2 BOX layer are determined by its breakdown voltage and leakage current, which are determined in this case by the quantities of generated defects and hydrogen content. They can be diminished completely only after very high temperature annealing, e.g., at 1100°C for more than 2 hours.

Secondly, in using a BOX layer in the above way, a thermal oxide boundary layer grows on the first wafer at the BOX layer. This thermal oxide boundary layer may be just a few nanometers thick but limits using such SOI structures for extremely thin devices with low dimension channels (nano field effect transistors, single electron transistors and quantum devices), where the boundary quality should be extremely high.

Thirdly, the need of using a relatively high energy H+ ion implantation to pass the oxide layer and exfoliating a thin silicon layer beneath leads to high straggling in the penetration distance of H+ ions, increased dose, defects in hydrogen content in the BOX, and increase in roughness of the exfoliated surface.

Fourthly, inhomogeneity in the exfoliated surface of the first wafer results due to starting the exfoliation at a few places at the high temperature .

Fifthly, hydrogen and other gas flatulence results from the micropores at the bonded interface.

Another known method for producing a silicon-on-insulator (SOI) structure (Invention of RF no. 2164719, IPC: ? 01 L 21/324) implants hydrogen ions in the first wafer, grows the thermal oxide on the second wafer, chemically treats the first and second wafers for their direct bonding, and exfoliates the first wafer with following removal of any damaged surface layer on the SOI structure. The thermal oxide has a thickness of 0.2-0.5 μm. The hydrogen implantation is carried out through the thermal oxide (SiO_2) layer (20 - 50 nm) that is deleted by etching after the implantation with a dose of H_2^+ ions (2.5-5) $x10^{16}cm^{-2}$. Direct bonding of the wafers is carried out in the air at 150-250°C during 1-2 hours. Exfoliation of the first wafer is provided with annealing at 350-450°C during 0.5-2 hours. High temperature annealing at 1100°C during 0.5-1 hour is used for complete defect removing. Subsurface damage is removed by touch polishing after previous oxidation and etching.

This known technical solution also has disadvantages that diminish the quality of silicon-on-insulator wafers. They include:

firstly, hydrogne pores at the bond interface created by residual impurities physically adsorbed at the surfaces bonded with following flaking due to hydrogen release during high temperature treatment; and

secondly, the thermal treatment at 350°C, which coincides with the beginning of detrapping hydrogen from the hydrogen filled pores, causes an inhomogeneous silicon layer and a rough surface on the final SOI .

SUMMARY OF THE INVENTION

The technical result of the invention is an improvement of quality of SOI structure.

The technical result is reached in that hydrogen implantation is carried out in the first wafer, the thermal oxide is grown on the second wafer, and the first and second wafers are treated chemically. Then, after chemical treatment, drying, removing of physically adsorbed substances from the wafer surfaces, joining the wafers, their splicing and exfoliating of the first wafer are carried out in a low vacuum at one or more temperatures at which the implanted hydrogen remains in a bound state.

Preferably, the hydrogen implantation is carried out through a thin (5 - 50 nm) thermal SiO_2 layer, which is removed after the implantation.

Preferably, H_2^+ or H^+ ions are used with the doses (1.5-15) $x10^{16}$ cm^{-2} and energies of 20-200 keV.

Preferably, the thermally grown oxide thickness on the second wafer is equal to 0.01-3 μm.

Preferably, high temperature annealing is carried out at 1100°C during 0.5-1 hour.

Preferably, a subsurface damaged layer in the silicon-on-insulator structure, obtained in exfoliating the hydrogen implanted layer inside the silicon wafer, is removed by oxidation, etching and touch polishing.

Preferably, the thermal oxide is grown before the thermal treatment.

According to another preferable variant, a glass wafer is used as a substrate with the thickness near 500 μm.

According to a more preferable variant, a quartz wafer is used as a substrate with

the thickness near 500 μm.

According to a most preferable variant, drying, removing physically adsorbed substances from the first and second wafer surfaces, joining the wafers, their splicing and exfoliating of the first wafer are carried out in the low vacuum (10^1 - 10^4 Pa) at the temperature interval from 80° to 350°C with duration from 0.1 to 100 hours.

BRIEF DESCRIPTION OF THE DRAWINGS

The substance of the invention is explained by the following description and enclosed figures.

The stage of hydrogen implantation for producing the SOI structure by the claimed method is presented in Fig.1.

The stage of drying, removing of the physically adsorbed substances from the first wafer and substrate surfaces, joining the wafers, their splicing and exfoliating of the first wafer for obtaining a thin silicon film in the low vacuum chamber are presented in Fig.2.

A photo of the surface of a SOI structure produced at atmospheric pressure is presented in Fig.3.

A photo of the surface of a SOI structure produced at low pressure conditions is presented in Fig.4.

An atomic force microscopy (AFM) image of the surface roughness (root mean square roughness ~ 11.3 nm) of a SOI structure produced by H^+ ion implantation with energy of 100 keV is presented in Fig.5.

An atomic force microscopy (AFM) image of the surface roughness (root mean

square roughness ~ 6.7 nm) of a SOI structure produced by H^+ ion implantation with energy of ~20 keV is presented in Fig.6.

A photo of the surface of a SOI structure produced by the claimed method is presented in Fig.7 to show there aren't microblisters or micropipes with dimensions larger than 0.25 μm on the surface of the SOI wafer.

DETAILED DESCRIPTION OF THE INVENTION

A physical basis of the method is a difference in the surface energies of the hydrophilic Si/SiO_2 and Si/Si surfaces in different temperature intervals. Particularly, the surface energy of the hydrophilic surfaces Si/SiO_2 is larger than the surface energy of the hydrophobic surfaces Si/Si at the temperatures 20 - 500°C. This can be as high as one order of magnitude at the temperature interval 150 - 300°C. It should be mentioned that these temperatures are lower than the temperatures that were used for splicing and transferring of the thin film of silicon and silicon dioxide layers by the known method for producing SOI wafers (US patent no. 5 374 564, IPC: 5 H01L 21/265), which are equal to ~500°C on reasoning from the conditions for hydrogen release from the connected states and transition into micropores for increased inside pressure. These conditions are necessary for the exfoliation of first wafer along the implanted layer.

In the present method, the SOI structure can be considered as a joining the hydrophilic surfaces (splicing) and the break up of the hydrophobic bonds at the inner surfaces (hydrogen induced thin film transfer) at the temperatures indicated. Therefore, two

main tasks should be solved. Firstly, high performance outer hydrophilic surfaces should be produced. Secondly, inner hydrophobic surfaces inside the silicon wafer should be created.

Parameters that determine of the surface energy in each case are the temperature and the structural quality of the surfaces. That raises the need for extremely high cleanness. The splicing surfaces must be without physically adsorbed impurities for 100% bonding. Standard RCA cleaning procedure (Semiconductor Wafer Bonding. Science and Technology, Q.-Y. Tong, U. Gosele, John Wiley & Sons, Inc., New York, NY, 10158-0012, p. 52) were used for reaching the needed cleanness. This consisted of ammonia-peroxide solution, etching of natural oxide by diluted hydrofluoric acid and final treatment in the peroxide-acid solution. Rinsing in ultra pure deionized water was used after each treatment. Wafer bonding was carried out between hydrophilic surfaces obtained by such treatment at different ratios (RCA-1, RCA-2), which provides contact angles for silicon and silicon dioxide from 0 to 10° (Semiconductor Wafer Bonding. Science and Technology, Q.-Y. Tong, U. Gosele, John Wiley & Sons, Inc., New York, NY, 10158-0012, p. 62). The wafers were placed in a centrifuge inside a low vacuum chamber for drying and removing of physically adsorbed substances from the first wafer and substrate surfaces, heated up to 80 - 350°C and then bonded together.

Inner hydrophobic surfaces in atomic planes parallel to the wafer surface can be formed by hydrogen implantation. Their formation takes place by the constitution of Si-H-H-Si bonds in this layer due to trapping of hydrogen atoms on the stretched and weakened Si-Si bonds that are perpendicular to the surface. In order to form two hydrophobic (100) planes with 100% covering by Si-H-H-Si bonds, the dose of H^+ ions

with energies 20 - 200 keV should be at least $3x10^{17}$ cm^{-2} or higher. But even at a dose of ~1,5 x 10^{16} cm^{-2} and energy of ~20 keV, microcracks start to appear inside the implanted layer. Their presence weakens the Si-Si bonds in the implanted layer with surface energies close to the hydrophobically bonded silicon surfaces. But as there is no need for 100% Si-H-H-Si bonds at the inner surfaces. Starting from this consideration, the invention chooses hydrogen doses from $1.5x10^{16}$ to $1.5x10^{17}$ cm^{-2} for ion energies 20 - 200 keV, respectively.

The technical result was obtained by the major stages presented in Fig.1 and 2.

1. Hydrogen ion implantation is carried out at the first major stage (Fig.1) in the first wafer 1 with ion energies 20 - 200 keV through a thin SiO2 layer (5-50 nm), which prevents the surface contamination, to provide a hydrogen implanted layer 2. The hydrogen dose needed for exfoliation of thin silicon film at the following thermal treatment stage is $1.5x10^{16}$ - $1.5x10^{17}$ cm^{-2} for ion energies 20 - 200 keV, respectively.

2. The oxide layer 4, which will be the buried oxide after bonding of the silicon wafer 1, is grown thermally on the second, substrate wafer 3, which is not irradiated by ions to keep its high quality in SOI structure.

3. Chemical treatment of the wafer 1 and the substrate 3 for cleaning and hydrophilisation followed by water stream douche or ultrasonic deionized water stream is carried out using peroxide-acid and ammonia-peroxide solutions with different ratios $NH_4OH:H_2O:H_2O$ = 1:1:5 - 1:2:7 and $HCl:H_2O_2:H_2O$ = 1:1:6 - 1:2:8 (RCA-1 and RCA-2, respectively).

4. Drying, removing of physically adsorbed substances from the surfaces of the

wafer 1 and substrate 3, joining the wafer 1 and substrate 3, their splicing and exfoliating along the implanted layer 2 in the wafer 1 at the temperatures 80 - 350°C with duration from 0.1 to 100 hours in the same low vacuum chamber (10^1 - 10^4 Pa) are carried out at the second major stage (Fig.2).

5. Concluding high temperature annealing is carried out at 1100°± 50°C during 0.5-1 hour. This is needed in some cases for increasing the bonding energies between the silicon wafer 1 and the substrate 3 to the value of breaking energy for the bulk silicon, as well as for removing residual radiation defects and hydrogen atoms from the exfoliated silicon layer.

6. Touch polishing or oxidation with following etching is carried out for removing any damaged upper layer 5 of exfoliated silicon film.

Thus, the main difference of the method for producing a SOI structure by hydrogen-induced transfer is that drying, removing of the of physically adsorbed substances from the surfaces of the wafers, joining the wafer and substrate, their splicing and exfoliating along the implanted layer in the wafer at the temperatures 80 - 350°C with duration from 0.1 to 100 hours are carried out in one stage in the same low vacuum chamber (10^1 - 10^4 Pa) (Fig.2). SOI structures produced at the low vacuum conditions have a higher quality, which is manifested in the absence of microblisters and micropipes that is demonstrated by Fig.4 in comparison with the SOI structure obtained at atmosphere conditions presented in Fig.3. An increase in the bonding energy between the wafer and substrate decreases the implantation energy, the thickness of the transferred layer, the roughness of the SOI wafer surface (Fig.6) as well as the total radiation-thermal impact on the structure used for producing the SOI in comparison with the roughness of SOI wafer

surface produced by hydrogen ions with higher energy (Fig.5).

The examples of specific realizations are presented below for more exact understanding of the invention.

Example 1.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 140 keV and dose $2.5x10^{16}$ cm^{-2} through a thin 50 nm SiO_2 layer, which prevents surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 (280 nm) is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by peroxide-acid and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 300°C, dried and cleaned from the physically adsorbed substances during 0.1 hour and then joined together, spliced and exfoliated along the implanted layer at the same conditions during 40 hours. In the result spontaneous exfoliation occurs and the final SOI structure appears with 0.6 μm Si / 0.28 mm SiO_2 / Si substrate. The photo of the surface produced is presented as Fig.7, which demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of SOI wafer.

5. Touch chemical-mechanical polishing (CMP) is carried out for removing of upper damaged layer on the surface of exfoliated silicon film in SOI structure.

Example 2.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 40 keV and dose 1 ,5x10^{16} cm^{-2} through thin 5 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 (280 nm) is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^1 Pa and heated to the temperature 200°C, dried and cleaned from physically adsorbed substances during 0.15 hour, then joined together and heated to 300°C, spliced and exfoliated along the implanted layer at the same conditions during 40 hours. In the result spontaneous exfoliation occurs and the final SOI structure appears with 0.2 μm Si / 0.28 μm SiO_2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of SOI wafer.

5. Thermal oxidation and chemical etching in diluted hydrofluoric acid is carried out

for removing of upper damaged layer on the surface of exfoliated silicon film of the SOI structure.

Example 3.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 140 keV and dose $5x10^{16}$ cm^{-2} through thin 50 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 with the thickness 280 nm is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 150°C, dried and cleaned from physically adsorbed substances during 0.2 hour, then joined together and heated to 300°C, spliced and exfoliated along the implanted layer at the same conditions during 10 hours, then the joined wafer and substrate are removed from low vacuum chamber and are exfoliated mechanically in the air, and the final SOI structure appears with 0.6 μm Si / 0.28 μm SiO_2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25

μm on the surface of the SOI wafer.

5. Thermal treatment of SOI structure at the temperature 1100°C during 1 hour is carried out for removing of the rest defects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing upper rough layer on the surface of exfoliated silicon film in the SOI structure.

Example 4.

1. H^+ ion implantation is carried out in silicon wafer with ion energy 20 keV and dose $4x10^{16}$ cm^{-2} through thin 5 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 with the thickness 10 nm is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 300°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together and heated to 300°C, spliced and exfoliated along the implanted layer at the same conditions during 40 hours. In the result spontaneous exfoliation occurs and the final SOI

structure appears with 0.2 μm Si / 0.28 μm SiO2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 mm on the surface of the SOI wafer.

5. Thermal oxidation and chemical etching in diluted hydrofluoric acid is carried out for removing upper damaged layer on the surface of exfoliated silicon film in the SOI structure.

Example 5.

1. H^+ ion implantation is carried out in silicon wafer with ion energy 200 keV and dose $1.5x10^{17}$ cm^{-2} through thin 50 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 with the thickness 410 nm is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^4 Pa and heated to the temperature 350°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together, spliced and exfoliated along the implanted layer at the same conditions during 5

hours. In the result spontaneous exfoliation occurs and the final SOI structure appears with 1.8 μm Si / 0.41 μm SiO_2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 mm on the surface of the SOI wafer.

5. Thermal oxidation and chemical etching in diluted hydrofluoric acid is carried out for removing of upper damaged layer on the surface of exfoliated silicon film in the SOI structure.

Example 6.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 140 keV and dose $6x10^{16}$ cm^{-2} through thin 50 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 with the thickness 280 nm is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 80°C, dried and cleaned from the physically adsorbed substances during 1 hour, then joined

together and heated to 300°C, spliced and exfoliated along the implanted layer at the same conditions during 25 hours. In the result spontaneous exfoliation occurs, and the final SOI structure appears with 0.6 μm Si / 0.28 μm SiO_2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of the SOI wafer.

5. Thermal treatment of SOI structure at the temperature 1100°C during 1 hour is carried out for removing defects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing of upper rough layer on the surface of exfoliated silicon film in the SOI structure.

Example 7.

1. H^+ ion implantation is carried out in silicon wafer with ion energy 20 keV and dose $4x10^{16}$ cm^{-2} through thin 5 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Silicon wafer with grown thermal oxide SiO_2 with the thickness 3.0 μm is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are

placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 350°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together, spliced and exfoliated along the implanted layer at the same conditions during 10 hours. In the result spontaneous exfoliation occurs, and the final SOI structure appears with 0.2 μm Si / 3.0 μm SiO_2 / Si substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of the SOI wafer.

5. Thermal treatment of SOI structure at the temperature 900°C during 1 hour is carried out for removing defects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing of upper rough layer on the surface of exfoliated silicon film in the SOI structure.

Example 8.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 140 keV and dose $3.5x10^{16}$ cm^{-2} through thin 50 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Glass (type LK-5 or Pyrex) wafer with the thickness 500 μm after CMP is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water

stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 300°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together, spliced and exfoliated along the implanted layer at the same conditions during 30 hours. In the result spontaneous exfoliation occurs, and the final SOI structure appears with 0.6 μm Si / 500 μm SiO_2 glass substrate. The investigation of the surface for produced SOI structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of silicon-on-glass (SOG) wafer.

5. Thermal treatment of SOG structure at the temperature 650°C during 10 hours is carried out for removing defects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing upper rough layer on the surface of exfoliated silicon film in the SOG structure.

Example 9.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 140 keV and dose 3.5×10^{16} cm^{-2} through thin 50 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Glass (type LK-5 or Pyrex) wafer with the thickness 500 μm after CMP is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream

and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^3 Pa and heated to the temperature 350°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together with applying the electric field them (negative electrode is placed at the glass), spliced and exfoliated along the implanted layer at the same conditions during 30 hours. In the result spontaneous exfoliation occurs, and the final structure appears with 0.6 μm Si / 500 μm SiO_2 glass substrate. The investigation of the surface for produced structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of silicon-on-glass (SOG) wafer.

5. Thermal treatment of SOG structure at the temperature 650°C during 10 hours is carried out for removing defects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing upper rough layer on the surface of exfoliated silicon film in the SOG structure.

Example 10.

1. H_2^+ ion implantation is carried out in silicon wafer with ion energy 40 keV and dose 2.5×10^{16} cm^{-2} through thin 5 nm SiO_2 layer, which prevents the surface contamination and then is removed.

2. Quartz wafer with the thickness 500 μm after CMP is used as a substrate.

3. Chemical treatment of implanted silicon wafer and substrate is carried out including cleaning with deionized water stream douche or ultrasonic deionized water stream and hydrophilisation of surfaces of implanted wafer and unimplanted substrate, using treatment by RCA and ammonia-peroxide solutions with following cleaning by water stream douche or ultrasonic deionized water stream.

4. H_2^+ ion implanted silicon wafer and silicon wafer with grown thermal oxide are placed in low vacuum chamber with pressure 10^2 Pa and heated to the temperature 300°C, dried and cleaned from the physically adsorbed substances during 0.1 hour, then joined together, spliced at the same conditions during 30 hours and cooled to room temperature. During cooling spontaneous exfoliation occurs, and the final structure appears with 0.6 μm Si / 500 μm quartz substrate. The investigation of the surface for produced structure demonstrates the absence of microblisters and micropipes with dimensions larger than 0.25 μm on the surface of silicon-on-quartz (SOQ) wafer.

5. Thermal treatment of SOQ structure at the temperature 650oC during 10 hours is carried out for removingdefects and hydrogen atoms.

6. Touch chemical-mechanical polishing (CMP) is carried out for removing upper rough layer on the surface of exfoliated silicon film in the SOQ structure.

As seen from the examples, the method for producing silicon-on-insulator structures using drying, removing of the of physically adsorbed substances from the surfaces of the wafers, joining the wafer and substrate, their splicing and exfoliating (hydrogen induced transferring along the implanted layer in the wafer) in the low vacuum conditions at the

moderate temperatures allows in comparison with known technical solutions:

1. decrease of needed ion energy and thickness of transferred (exfoliated) layer;

2. decrease of needed hydrogen ion dose and irradiation time;

3. decrease of roughness of SOI structure surface as well as total radiation-thermal impact on the structures used for SOI production;

4. decrease of defect concentration at the grain boundary Si/SiO_2;

5. practically full absence of microblisters on the SOI surface and micropipes in the silicon film;

6. increase of quality and yield of suitable SOI wafers; and

7. reduction of cost of SOI structures due to absence of slicing (exfoliating) procedure at the temperatures 400-600°C .

These advantages are the consequence of desorption of water and other physically adsorbed substances from the surfaces of joined wafers at moderate heating in low vacuum conditions and also the consequence of a few orders of magnitude decrease in the gas quantity trapped at the micropores between the joined wafers that leads during further thermal treatment to micorbubles (microblisters) and microcraters (micropipes) in a cut off silicon layer of SOI structure.

Industrial Applicability

The invention can be used in producing materials for microelectronics and, particularly, silicon-on-insulator structures (SOI) of ultra large scale integrated circuits and other microelectrinc devices.